

# Claims

[c1] What is claimed is:

1. A method for Peripheral Component Interconnect (PCI) Express Power Management (PM) using a PCI PM mechanism in a computer system, the computer system including a PCI Power Management Event (PME) controller and a PCI Express Root Complex, the method comprising:  
converting a plurality of PM\_PME packets generated by the PCI Express Root Complex into a Pseudo-PME signal, a first PM\_PME packet of the plurality of PM\_PME packets asserting the Pseudo-PME signal so that a voltage of Pseudo-PME signal changes from a first level to a second level;  
providing a Pseudo-PME line electrically connected to a PME input of the PCI PME controller and the PCI Express Root Complex for transmitting the Pseudo-PME signal to the PCI PME controller, the PME input receiving PME signals generated by PCI-compliant devices through a PCI Bus of the computer system; and  
de-asserting the Pseudo-PME signal so that the voltage of the Pseudo-PME signal changes from the second level to the first level, the de-assertion of the Pseudo-PME signal following the assertion of the Pseudo-PME signal

by a predetermined time interval;  
wherein the first level and the second level of the voltage  
of the Pseudo-PME signal are PCI-compliant.

- [c2] 2.The method of claim 1 wherein the PCI PME controller  
is a chipset of the computer system.
- [c3] 3.The method of claim 1 further comprising providing a  
sequential circuit to convert the PM\_PME packets into the  
Pseudo-PME signal.
- [c4] 4.The method of claim 3 wherein the sequential circuit is  
a latch or a flip-flop.
- [c5] 5.The method of claim 1 further comprising providing a  
timer to control a time interval between asserting and  
de-asserting the Pseudo-PME signal.
- [c6] 6.The method of claim 1 further comprising converting a  
pulse of a PM\_PME packet of the plurality of PM\_PME  
packets into a lower frequency pulse to control a time  
interval between asserting and de-asserting the Pseudo-  
PME signal.
- [c7] 7.The method of claim 6 further comprising providing a  
synchronizer to convert the pulse of the PM\_PME packet  
of the plurality of PM\_PME packets into the lower fre-  
quency pulse.

- [c8] 8. The method of claim 6 wherein the lower frequency pulse is an active-low pulse and works as the Pseudo-PME signal in the computer system.
- [c9] 9. The method of claim 1 wherein the PCI PME controller includes an event register which can be set by the PCI PME controller when the Pseudo-PME signal is asserted but cannot be cleared when the Pseudo-PME signal is de-asserted, the method further comprises clearing the event register with a program of the computer system.
- [c10] 10. The method of claim 9 wherein the program is a device driver of the computer system.
- [c11] 11. A computer system comprising:
  - a PCI Express Root Complex for generating a plurality of PM\_PME packets;
  - a sequential circuit electrically connected to the PCI Express Root Complex for converting the plurality of PM\_PME packets into a Pseudo-PME signal;
  - a PCI PME controller comprising an event register, the event register for reporting a power management event to the computer system;
  - a Pseudo-PME line electrically connecting an output of the sequential circuit to a PME input of the PCI PME controller, the event register being cleared when the

Pseudo-PME signal changes from a first level to a second level; and

a memory comprising computer code executed by the computer system when voltage of the Pseudo-PME signal changes from the second level to the first level, the computer code capable of clearing the event register; wherein the first level and the second level of the voltage of the Pseudo-PME signal are PCI-compliant.

[c12] 12. The computer system of claim 11 further comprising a timer connected to the sequential circuit to control when voltage of the Pseudo-PME signal is changed from the second level to the first level.